Datasheet

IMPINJ MONZA R6

TAG CHIP DATASHEET

IPJ-W1700-K00

Version 7.0

www.impinj.com

OVERVIEW

The Monza® R6 UHF RFID tag chip is optimized for serializing items such as apparel, electronics, cosmetics, documents and jewelry. It delivers unmatched read performance and data integrity for effective RFID business systems and record-breaking encoding performance to enable the lowest applied tag cost.

The Monza R6 tag chip includes revolutionary technologies such as automatic performance adjustments and encoding diagnostics that reinforce the position of the Monza tag chip family as the RFID industry leader.

FEATURES

- Industry leading read sensitivity of up to -22.1 dBm with a dipole antenna, combined with excellent interference rejection, delivers exceptional read reliability
- Superior write sensitivity of up to -18.8 dBm with a dipole antenna for unparalleled encoding reliability
- Inlay compatibility between all Monza 6 family of tag chips
- Fast memory write speed of 1.6 ms for 32 bits
- Encoding throughput up to 9,500 tags/minute using the Impinj STP® source tagging platform
- Up to 96 bits of EPC memory
- 96 bits of Serialized TID with 48-bit serial number
- EPCglobal and ISO 18000-63 compliant, Gen2v2 compliant
- Unmatched data integrity with Integra™ Technology for encoding diagnostics
- Maintains performance across different dielectrics with AutoTune™ Technology
- Reduced tag manufacturing variability via Enduro™ Technology
- FastID™ mode enables 2x to 3x faster EPC+TID inventory for authentication and other TID-based applications
- TagFocus™ mode suppresses previously read tags to enable capture of more tags
- Scalable serialization built-in with Monza Self-Serialization
- Impinj's field-rewritable NVM, optimized for RFID, provides 100,000 cycle or 50-year retention reliability

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1 INTRODUCTION

1.1 Scope

This datasheet defines the physical and logical specifications for Gen2-compliant Monza R6 tag silicon, a reader-talks-first, radio frequency identification (RFID) component operating in the UHF frequency range.

1.2 Reference Documents

The following reference documents were used to compile this datasheet:

- EPC™ Radio Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz (Gen2 Specification)
  - The conventions used in the Gen2 Specification (normative references, terms and definitions, symbols, abbreviated terms, and notation) were adopted in the drafting of this Monza R6 Tag Chip Datasheet. Users of this datasheet should familiarize themselves with the Gen2 Specification.
- Impinj Monza R6 Wafer Specification
- Impinj Monza Wafer Map Orientation
- EPC™ Tag Data Standards Specification 1.7
- EPCglobal "Interoperability Test System for EPC Compliant Class-1 Generation-2 UHF RFID Devices" v.1.2.4, August 4, 2006
  - Monza R6 tag chips are compliant with this Gen2 interoperability standard.

You may consult these documents for more information about compliance standards and specifications.

2 FUNCTIONAL DESCRIPTION

The Monza R6 tag chip fully supports all requirements of the Gen2 specification as well as many optional commands and features (see Support for Optional Gen2 Commands, section 2.3). In addition, the Monza tag chip family provides a number of enhancements:

- Superior sensitivity for high read and write reliability
- Industry-leading memory write speed, delivering the highest encoding rates
- TagFocus™ inventory mode, a Gen2 compliant, patented method for capturing more hard-to-read tags by suppressing those that have already been read, by extending their S1 flag B-state
- FastID™ inventory mode, a Gen2 compliant, patented method for EPC+TID based inventory that is 2-3 times faster than previous methods
- A patented Enduro™ technology makes inlay manufacture less sensitive to die-attach pressure, resulting in less variance and more predictable performance in final inlay product.
- AutoTune™ technology allows Monza R6 inlays to maintain high performance independent of the tagged items dielectric. In addition, smaller form factor designs can meet bandwidth requirements with AutoTune. Smaller antennas reduce manufacturing cost and increase the number of applications.
- Integra™ technology, a suite of diagnostics which ensures consistently accurate data delivery that business can depend on

2.1 Memory

Optimized for item-level tagging, Monza R6 tag chips offer EPC memory of up to 96 bits, serialized TID. Monza R6 does not have any user programmable passwords. As per the Gen2 specifications the

passwords are PermaReadLocked and set to zero. It follows that Monza R6 is not killable and does not utilize the *Access* command. See Table 1 for the memory organization.

Table 1: Monza R6 Memory Organization

MEMORY SECTION	DESCRIPTION
User	None
TID (not changeable)	Serial Number—48 bits
	Extended TID Header—16 bits
	Company/Model Number—32 bits
EPC	Up to 96 bits
Reserved	AutoTune Disable and Readout
	Kill password - None
	Access password - None

2.2 Advanced Monza Features Support More Effective Inventory

Monza tag chips support two unique, patented features designed to boost inventory performance for traditional EPC and TID-based applications:

- TagFocus™ mode minimizes redundant reads of strong tags, allowing the reader to focus on weak tags that are typically the last to be found. Using TagFocus, readers can suppress previously read tags by indefinitely refreshing their S1 B state.
- FastID™ mode makes TID-based applications such as authentication practical by boosting TID-based inventory speeds by 2 to 3 times. Readers can inventory both the EPC and the TID without having to perform an *Access* command. Setting the EPC word length to zero enables TID-only serialization.

2.3 Support for Optional Gen2 Commands

Monza R6 tag chips support the optional commands listed in Table 2.

Table 2: Supported Optional Gen2 Specification Commands

COMMAND	CODE	LENGTH (BITS)	DETAILS
BlockWrite	11000111	>57	• Accepts valid one-word commands • Accepts valid two-word commands if pointer is an even value • Returns error code (00000000_2) if it receives a valid two-word command with an odd value pointer • Returns error code (00000000_2) if it receives a command for more than two words • Does not respond to block write commands of zero words
Lock	11000101	60	• Monza R6 uses an alternative version of the lock command • There is only a single lock bit which is described in the Gen2 specification • To permalock all of the memory a *Lock* command must be sent with a payload of all ones $FFFFF_h$.

2.4 Data Integrity Features (Integra™ Technology)

Monza R6 has several data integrity features that enhance encoding and data reliability. These features include memory self-check, TID parity, and the *MarginRead* command.

2.4.1 Memory Self-Check

Monza R6 performs a memory check on its NVM at every power-up. If a bit is weakly encoded an internal flag is set. When the tag is singulated it will respond back with a zero length EPC. A reader could then consider this tag for exception handling.

2.4.2 TID Parity

Monza R6 is encoded with even parity over the 48-bit serial number portion of the TID. A reader should calculate even parity with bitwise exclusive-OR as follows.

- X = TID bit(30_h) ⊕ TID bit(31_h) ⊕ … ⊕ TID bit($5E_h$) ⊕ TID bit($5F_h$)
- If X = 0 the TID data is good
- If X = 1 the TID data has an error in it

Table 3, Table 4, and Table 5 provide details about the custom Impinj *MarginRead* command.

Table 3: MarginRead Command Code

COMMAND	CODE	LENGTH	DETAILS
MarginRead	1110000000000001	≥67	• The *MarginRead* command allows checking for sufficient write margin of known data • The tag must be in the OPEN/SECURED state to respond to the command • If a tag receives a *MarginRead* command with an invalid handle, it ignores that command • The tag responds with the Insufficient Power error code if the power is too low to execute a *MarginRead* • The tag responds with the Other error code if the margin is bad for a bit in the mask or if a non-matching bit is sent by the reader • The *MarginRead* command is only applicable for programmable sections of the memory

Table 4: MarginRead Command Details

MARGINREAD COMMAND	CODE	MEM BANK	BIT POINTER	LENGTH	MASK	RN	CRC-16
#bits	16	2	EBV	8	Variable	16	16
Details	11100000 00000001	00: Reserved 01: EPC 10: TID 11: User	Starting Bit Address Pointer	Length in Bits	Mask Value	handle	

Table 5: MarginRead Command Field Descriptions

FIELD	DESCRIPTION
Mem Bank	The memory bank to access.
Bit Pointer	An EBV that indicates the starting bit address of the mask
Length	Length of the mask field from 1-255.
	A value of zero shall result in the command being ignored
Mask	This field must match the expected values of the bits
	The chip checks that each bit matches what is in the mask field with margin
RN	The tag will ignore any *MarginRead* command received with an invalid handle

The tag response to the *MarginRead* Command uses the preamble specified by the TRext value in the *Query* command that initiated the round. See Table 6 for tag response details.

Table 6: Tag Response to a Passing MarginRead Command

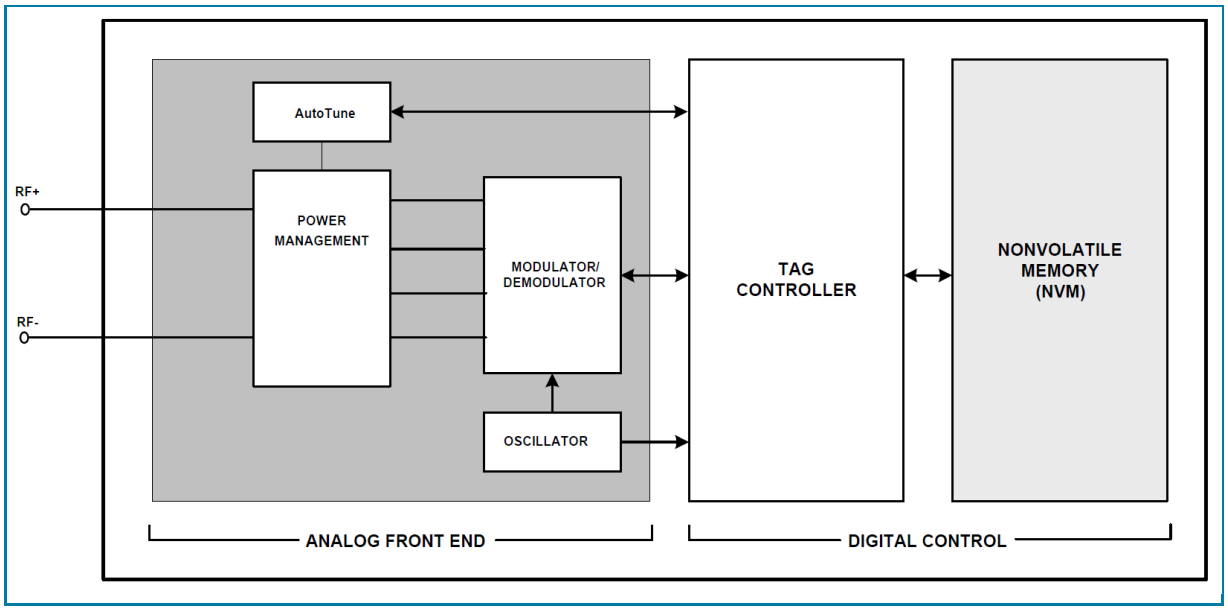
RESPONSE	HEADER	RN	CRC-16
#bits	1	16	16
Description	0	handle	

2.4.3 Recommended MarginRead Usage Guidelines

There are several ways that the *MarginRead* command could be used with Monza R6. Monza R6 comes pre-serialized and the *MarginRead* command allows a programming reader to check that the pre-serialized data is well written and does not need to be re-encoded. Another recommended use of *MarginRead* is secondary and independent verification of the encoding quality. *MarginRead* can also be used for diagnosis when doing failure analysis on tags. The *MarginRead* command obeys all locking and will return an error code on read locked passwords.

2.5 Monza R6 Tag Chip Block Diagram

Figure 1: Block Diagram



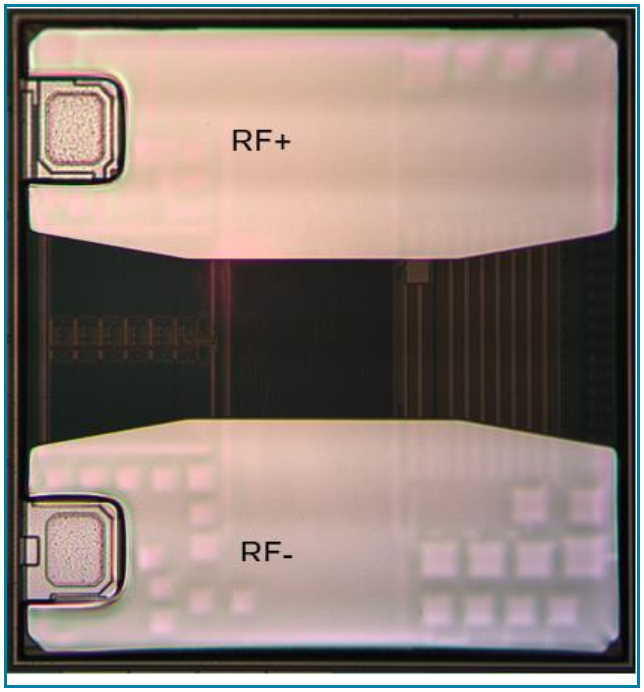
2.6 Pad Descriptions

Monza R6 tag chips have two external pads available to the user: one RF+ pad, and one RF- pads. RF+ and RF- form a single differential antenna port. See Table 7 (also see Figure 1 and Figure 2). Note that none of these pads connects to the chip substrate.

Table 7: Pad Descriptions

EXTERNAL SIGNALS	EXTERNAL PAD	DESCRIPTION
RF+	1	Differential RF Input Pads for Antenna.
RF-	2	

Figure 2: R6 Tag Chip Die Orientation



2.7 Monza 6 Antenna Reference Designs

All Monza 6 family of tag chips are designed to be drop-in compatible for antenna inlay designs. Impinj has a set of reference designs available for use by Monza customers under terms of the Impinj Antenna License Agreement.

These reference design documents are restricted. To access these documents, users must obtain access permission by creating an Impinj access account and submitting a request form through the Impinj Partner Access page[1]. Once Impinj has accepted their request, users can use their access credentials to view the Monza reference design documents page on the Support Portal[2].

2.8 Monza R6 Tag Chip Dimensions

The Monza R6 features a 464.1 µm x 400 µm rectangular die size.

2.9 Power Management

The tag is activated by proximity to an active reader. When the tag enters a reader's RF field, the Power Management block converts the induced electromagnetic field to the DC voltage that powers the chip.

2.10 AutoTune

The AutoTune block adjusts Monza R6 power harvesting from the inlay antenna by adjusting the chip's input capacitance. This adjustment occurs at power up and is held for the remainder of the time that Monza R6 is powered.

2.11 Modulator/Demodulator

The Monza R6 tag chip demodulates any of a reader's three possible modulation formats, DSB-ASK, SSB-ASK, or PR-ASK with PIE encoding. The tag communicates to a reader via backscatter of the incident RF waveform by switching the reflection coefficient of its antenna pair between reflective and absorptive states. Backscattered data is encoded as either FM0 or Miller subcarrier modulation (with the reader commanding both the encoding choice and the data rate).

2.12 Tag Controller

The Tag Controller block is a finite state machine (digital logic) that carries out command sequences and also performs a number of overhead duties.

2.13 Nonvolatile Memory

The Monza R6 tag chip embedded memory is nonvolatile memory (NVM) cell technology, specifically optimized for exceptionally high performance in RFID applications. All programming overhead circuitry is integrated on chip. Monza R6 tag chip NVM provides 100,000 cycle endurance or 50-year data retention.

The NVM block is organized into two segments:

- EPC Memory with up to 96 bits
- Reserved Memory (which contains the AutoTune Disable bit).

The ROM-based Tag Identification (TID) memory contains the EPCglobal class ID, the manufacturer identification, and the model number. It also contains an extended TID consisting of a 16-bit header and 48-bit serialization.

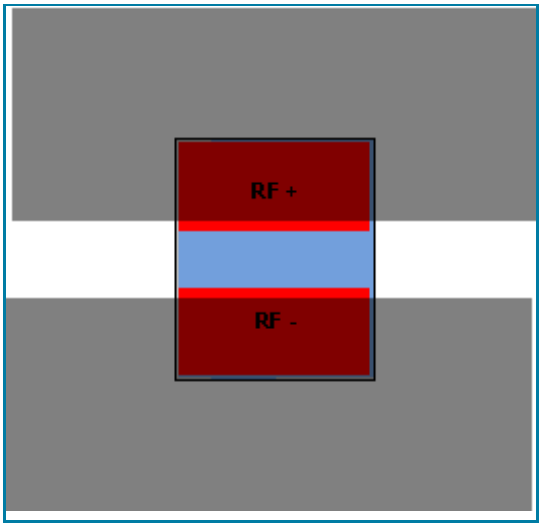
3 INTERFACE CHARACTERISTICS

This section describes the RF interface of the tag chip and the modulation characteristics of both communication links: reader-to-tag (Forward Link) and tag-to-reader (Reverse Link).

3.1 Making Connections

Figure 3 shows antenna connection for Monza R6 tag chips.

Figure 3: Antenna Connection for Inlay Production



This connection configuration for inlay production contacts the Monza R6 tag chip RF+ pad to one antenna terminal and the RF- pad to the opposite polarity terminal. Enduro pads allow relatively coarse antenna geometry, and thus enable relaxed resolution requirements for antenna patterning compared to bumped products. The diagram in Figure 3 shows the recommended antenna trace arrangement and chip placement – having antenna traces partially overlapping the Enduro pads but not extending into the clear space between Enduro pads.

3.2 Impedance Parameters

In order to realize the full performance potential of the Monza R6 tag chip, it is imperative that the antenna present the appropriate impedance at its terminals. A simplified lumped element tag chip model, shown in Figure 4, is the conjugate of the optimum source impedance, which is not equal to the chip input impedance. This indirect, source-pull method of deriving the port model is necessary due to the non-linear, time-varying nature of the tag RF circuits. The model is a good mathematical fit for the chip over a broad frequency range.

The lumped element values are listed in Table 8, where C_{mount} is the parasitic capacitance due to the antenna trace overlap with the chip surface, C_p appears at the chip terminals and is intrinsic to the chip, and R_p represents the energy conversion and energy absorption of the RF circuits.

Figure 4: Tag Chip Linearized RF Model

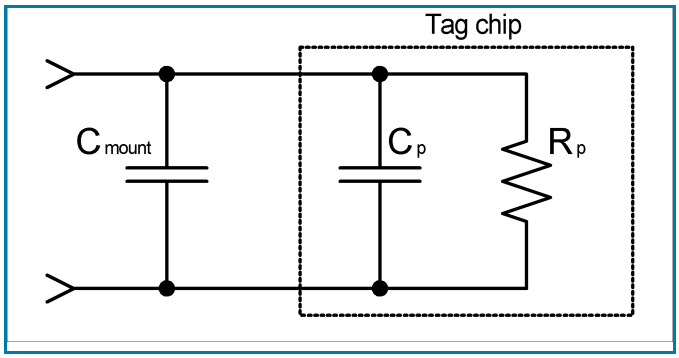


Table 8 shows the values for the chip port model for the Monza R6 tag chip, which apply to all frequencies of the primary regions of operation (North America, Europe, and Japan).

Table 8: R6 Chip Port Parameters

PARAMETER	TYPICAL VALUE	COMMENTS
C_p	1.23 pF	Intrinsic chip capacitance when AutoTune is mid-range, including Enduro pads.
R_p	1.2 kOhm	Calculated for linearized RF model shown in Figure 4. Measured R_p = 1.56 kOhm using network analyzer.
C_{mount}	0.21 pF	Typical capacitance due to adhesive and antenna mount parasitics. Total load capacitance presented to antenna model of Figure 4 is: $C_p + C_{mount}$
Chip Read Sensitivity	- 20 dBm	Measured at 25 °C; R=>T link using DSB-ASK modulation with 90% modulation depth, Tari=25 µs, and a T=>R link operating at 170 kbps with Miller M=8 encoding. Intrinsic chip capacitance when AutoTune is mid-range, including Enduro pads.
Chip Write Sensitivity	- 16.7 dBm	

3.3 Reader-to-Tag (Forward Link) Signal Characteristics

Table 9: Forward Link Signal Parameters

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	COMMENTS
RF Characteristics					
Carrier Frequency	860		960	MHz	North America: 902–928 MHz Europe: 865–868 MHz
Maximum RF Field Strength			+20	dBm	Received by a tag with dipole antenna while sitting on a maximum power reader antenna
Modulation		DSB-ASK, SSB-ASK, or PR-ASK			Double and single sideband amplitude shift keying; phase-reversal amplitude shift keying
Data Encoding		PIE			Pulse-interval encoding
Modulation Depth	80		100	%	(A-B)/A, A=envelope max., B=envelope min.
Ripple, Peak-to-Peak			5	%	Portion of A-B
Rise Time ($t_{r,10\text{-}90\%}$)	0		0.33Tari	sec	
Fall Time ($t_{f,10\text{-}90\%}$)	0		0.33Tari	sec	
Tari[1]	6.25		25	µs	Data 0 symbol period
PIE Symbol Ratio	1.5:1		2:1		Data 1 symbol duration relative to Data 0
Duty Cycle	48		82.3	%	Ratio of data symbol high time to total symbol time
Pulse Width	MAX(0.265Tari,2)		0.525Tari	µs	Pulse width defined as the low modulation time (50% amplitude)

3.4 Tag-to-Reader (Reverse Link) Signal Characteristics

Table 10: Reverse Link Signal Parameters

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	COMMENTS
Modulation Characteristics					
Modulation		ASK			FET Modulator
Data Encoding		Baseband FM0 or Miller Subcarrier			
Change in Modulator Reflection Coefficient $\|\Delta\Gamma\|$ due to Modulation		0.8			$\|\Delta\Gamma\| = \left\|\Gamma_{reflect} - \Gamma_{absorb}\right\|$ (per read/write sensitivity, Table 8)
Duty Cycle	45	50	55	%	
Symbol Period[1]	1.5625		25	µs	Baseband FM0
	3.125		200	µs	Miller-modulated subcarrier
Miller Subcarrier Frequency[1]	40		640	kHz	

NOTE: Values are nominal minimum and nominal maximum, and do not include frequency tolerance. Apply appropriate frequency tolerance to derive absolute periods and frequencies.

4 TAG MEMORY

4.1 Monza R6 Tag Chip Memory Map

Table 11: Gen2 Interface Memory Map

MEMORY BANK NUMBER	MEMORY BANK NAME	MEMORY BANK BIT ADDRESS	BIT ADDRESS															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10_2	TID (ROM)	50_h-$5F_h$	TID_Serial[15:0]															
		40_h-$4F_h$	TID_Serial[31:16]															
		30_h-$3F_h$	TID_Serial[47:32]															
		20_h-$2F_h$	Extended TID Header															
		10_h-$1F_h$	Manufacturer ID								Model Number							
		00_h-$0F_h$	1	1	1	0	0	0	1	0	Manufacturer ID							
01_2	EPC (NVM)	70_h-$7F_h$	EPC[15:0]															
		60_h-$6F_h$	EPC[31:16]															
		50_h-$5F_h$	EPC[47:32]															
		40_h-$4F_h$	EPC[63:48]															
		30_h-$3F_h$	EPC[79:64]															
		20_h-$2F_h$	EPC[95:80]															
		10_h-$1F_h$	Protocol-Control Bits (PC)															
		00_h-$0F_h$	CRC-16															
00_2	RESERVED (NVM)	$E0_h$-EF_h	RFU[12:0]=000_h													ATV[2:0]		
		50_h-$5F_h$	A	Factory Calibration B [14:0]														
		40_h-$4F_h$	Factory Calibration A [15:0]															
		30_h-$3F_h$	Access Password[15:0]=0000_h															
		20_h-$2F_h$	Access Password[31:16]=0000_h															
		10_h-$1F_h$	Kill Password[15:0]=0000_h															
		00_h-$0F_h$	Kill Password[31:16]=0000_h															

4.2 Logical vs. Physical Bit Identification

For the purposes of distinguishing most significant from least significant bits, a logical representation is used in this datasheet where MSBs correspond to large bit numbers and LSBs to small bit numbers. For example, Bit 15 is the logical MSB of a memory row in the memory map. Bit 0 is the LSB. A multi-bit word represented by WORD[N:0] is interpreted as MSB first when read from left to right. This convention should not be confused with the physical bit address indicated by the rows and column addresses in the memory map; the physical bit address describes the addressing used to access the memory.

4.3 Reserved Memory

Reserved Memory contains the Access and Kill passwords which are programmed to zero. It also contains the AutoTune disable bit, marked A in the memory map in Table 11, and the AutoTune value, marked ATV[2:0] in word 0xE. The AutoTune value represents the tuning capacitance scale, from zero to four. When the AutoTune disable bit is zero AutoTune works as normal. When the bit is one, AutoTune is disabled and the capacitance on the front end assumes the mid-range value.

4.3.1 Access Password

The Access Password is a 32-bit value stored in Reserved Memory 20_h to $3F_h$ MSB first. Monza R6 does not implement an Access Password and acts as though it has a zero-valued Access Password that is permanently read/write locked.

4.3.2 Kill Password

The Kill Password is a 32-bit value stored in Reserve Memory 00_h to $1F_h$, MSB first. Monza R6 does not implement a Kill Password and acts as though it has a zero-valued Kill Password that is permanently read/write locked.

4.3.3 PermaLock

To permalock all of the memory a *Lock* command must be sent with a payload of all ones, $FFFFF_h$.

4.3.4 AutoTune Disable and AutoTune Value

The AutoTune disable bit is the first bit in word 05_h, marked A in the memory map, and the AutoTune value, marked ATV[2:0] in word $0E_h$. The factory programmed value of the AutoTune disable bit is zero. The AutoTune value represents the tuning capacitance scale, from zero to four. A value of zero removes 100 fF of capacitance across the RF input of the tag and a value of four adds 100 fF across the RF input of the chip. See Table 12 for the mapping between AutoTune value and the change in input capacitance. A reader acquires the AutoTune value by issuing a single word *Read* command to word $0E_h$ in the reserved memory bank. The AutoTune value is not writable.

To disable AutoTune a reader issues a *Write* command or a single word *BlockWrite* command to word 05_h. Only the AutoTune disable bit will change and the rest of bits in the payload will be ignored. If the tag's memory is locked then the AutoTune disable bit will also be locked.

When the AutoTune disable bit is zero AutoTune works as normal and when the bit is one AutoTune is overridden and the capacitance across the RF input is set to 0 fF. When AutoTune is disabled, the readout of AutoTune value does not represent the value of capacitance across the RF input to the tag.

Table 12: AutoTune Value

AUTOTUNE VALUE	CHANGE IN INPUT CAPACITANCE (FF)
0h	-100
1h	-60
2h	0
3h	+60
4h	+100

4.4 EPC Memory (EPC Data, Protocol Control Bits, and CRC16)

As per the Gen2 specification, EPC memory contains a 16-bit cyclic-redundancy check word (CRC16) at memory addresses 00_h to $0F_h$, the 16 protocol-control bits (PC) at memory addresses 10_h to $1F_h$, and an EPC value beginning at address 20_h.

The protocol control fields include a five-bit EPC length, a one-bit user-memory indicator (UMI=0), a one-bit extended protocol control indicator (XI=0), and nine bits of memory from 17_h to $1F_h$ for the numbering system identifier (NSI) toggle bit, T, and Reserved for Future Use or Application Family Identifier (RFU or AFI), bits 18_h to $1F_h$. The factory default value is 3000_h.

On Monza R6 the EPC length may only be set to zero, two, four, or six which corresponds with the values of 0000_h, 1000_h, 2000_h, or 3000_h. Only the four MSB of the EPC length in the protocol-control bits may be programmedAll other protocol-control bits are non-programmable (read-only memory) and set to zero. Any attempt to write an unsupported length results in an unsupported EPC length field error code being backscattered.

The tag calculates the CRC16 upon power-up over the stored PC bits and the EPC specified by the EPC length field in the stored PC. For more details about the PC field or the CRC16, see the Gen2 specification.

A reader accesses EPC memory by setting MemBank = 01_2 in the appropriate command, and providing a memory address using the extensible-bit-vector (EBV) format. The CRC-16, PC, and EPC are stored MSB first (i.e., the EPC's MSB is stored in location 20_h).

The EPC memory bank of Monza R6 supports a maximum EPC size of 96 bits, which is the factory-programed EPC length. It is possible to adjust the EPC size down from 96 bits, according to the parameters laid out in the Gen2 standard. For Monza R6 chips (IPJ -W1700), the EPC value written into the chip during factory test is listed below in Table 13. The "X" nibbles in the pre-programmed EPC are pre-serialized values that follow the Impinj Monza Self-Serialization formula for Monza R6.

For more details on the pre-serialization formula used to generate the factory-programmed EPC, refer to the Monza TID Memory Maps for Self-Serialization[3].

Table 13: EPC at Factory-Program

IMPINJ PART NUMBER	EPC VALUE PRE-PROGRAMMED AT THE FACTORY (HEX)
IPJ-W1700	E280 1160 XXXX XXXX XXXX XXXX

4.5 Tag Identification (TID) Memory

The ROM-based Tag Identification memory contains Impinj-specific data. The Impinj MDID (Manufacturer Identifier) for Monza R6 is 100000000001; the location of the manufacturer ID is shown in the memory map tables in the Monza R6 Tag Chip Memory Map, section 4.1, and the bit details are given in Table 14. Note that a logic 1 in the most significant bit of the manufacturer ID (as in the example bordered in solid black in the table) indicates the presence of an extended TID consisting of a 16-bit header and a 48-bit serialization. The 48-bit serialization has even parity as discussed in TID Parity, section 2.4.2. The Monza R6 tag chip model number is located in the area bordered by the dashed line in TID memory row 10_h-$1F_h$ as shown in Table 14. The non-shaded bit locations in TID row 00_h-$0F_h$ store the EPCglobal™ Class ID (0xE2).

Table 14: TID Memory Details

MEMORY BANK NUMBER	MEMORY BANK NAME	MEMORY BANK BIT ADDRESS	BIT ADDRESS															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10_2	TID (ROM)	50_h-$5F_h$	TID_SERIAL[15:0]															
		40_h-$4F_h$	TID_SERIAL[31:16]															
		30_h-$3F_h$	TID_SERIAL[47:32]															
		20_h-$2F_h$	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
		10_h-$1F_h$	0	0	0	1	*Monza R6 Model Number*											
							0	0	0	1	0	1	1	0	0	0	0	0
		00_h-$0F_h$	1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0

4.6 User Memory

Monza R6 contains no user memory bank.

5 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed in this section may cause permanent damage to the tag. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this datasheet is not guaranteed or implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 Temperature

Several different temperature ranges will apply over unique operating and survival conditions. Table 15 lists the ranges that will be referred to in this specification. Tag functional and performance requirements are met over the operating range, unless otherwise specified.

Table 15: Temperature Parameters

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	COMMENTS
Extended Operating Temperature	–40		+85	°C	Default range for all functional and performance requirements
Storage Temperature	–40		+85/125	°C	At 125°C data retention is 1 year
Assembly Survival Temperature			+260	°C	Applied for one minute
Temperature Rate of Change			4	°C / sec	During operation

5.2 Electrostatic Discharge (ESD) Tolerance

The tag is guaranteed to survive ESD as specified in Table 16.

Table 16: ESD Limits

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	COMMENTS
ESD			2,000	V	HBM (Human Body Model)

5.3 NVM Use Model

Tag memory is designed to endure 100,000 write cycles or retain data for 50 years.

6 ORDERING INFORMATION

Contact sales@impinj.com for ordering support.

Table 17: Ordering Information

PART NUMBER	FORM	PRODUCT	PROCESSING FLOW
IPJ-W1700-K00	Wafer	Monza R6 tag chip	Padded, thinned (to ~109 µm), and diced

7 EXTERNAL REFERENCES

[1] Support Link: *Impinj Restricted Access Request Form* (https://access.impinj.com/prtlaccessrequest)

[2] Support Link: *Monza Reference Design Documents & Downloads* (https://support.impinj.com/hc/en-us/sections/200454558-Monza-Reference-Design-Documents-Downloads) – Note: These documents are restricted and require access permission from Impinj.

[3] Support Link: *TID Memory Maps for Monza Self-Serialization* (https://support.impinj.com/hc/en-us/articles/203444983-TID-Memory-Maps-for-Monza-Self-Serialization)

8 NOTICES

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